

FIG. 1

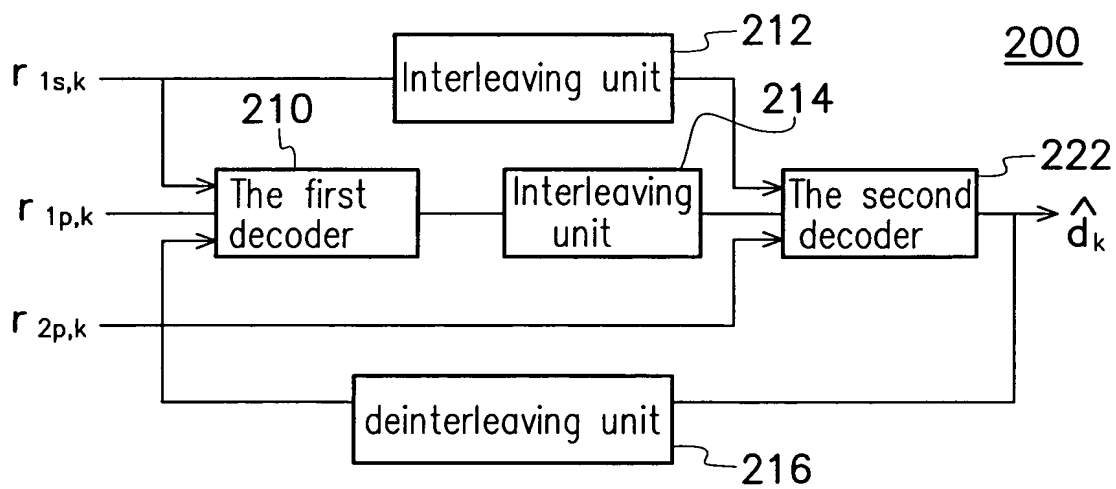


FIG. 2

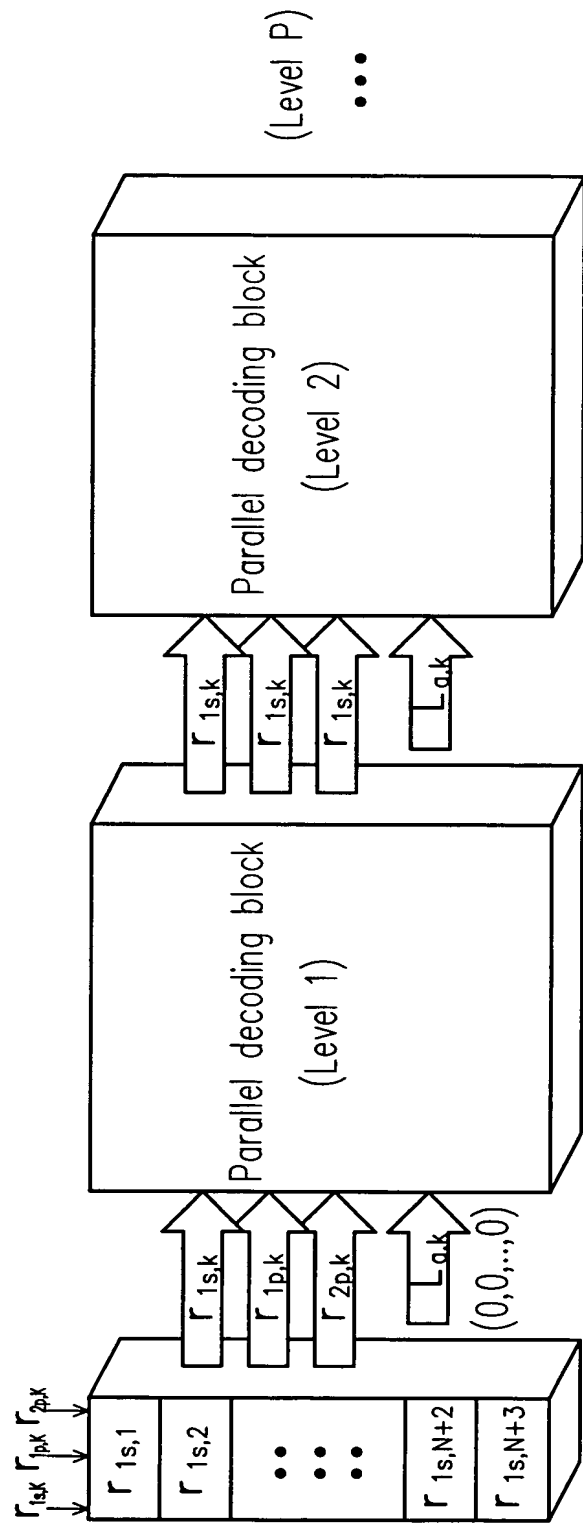
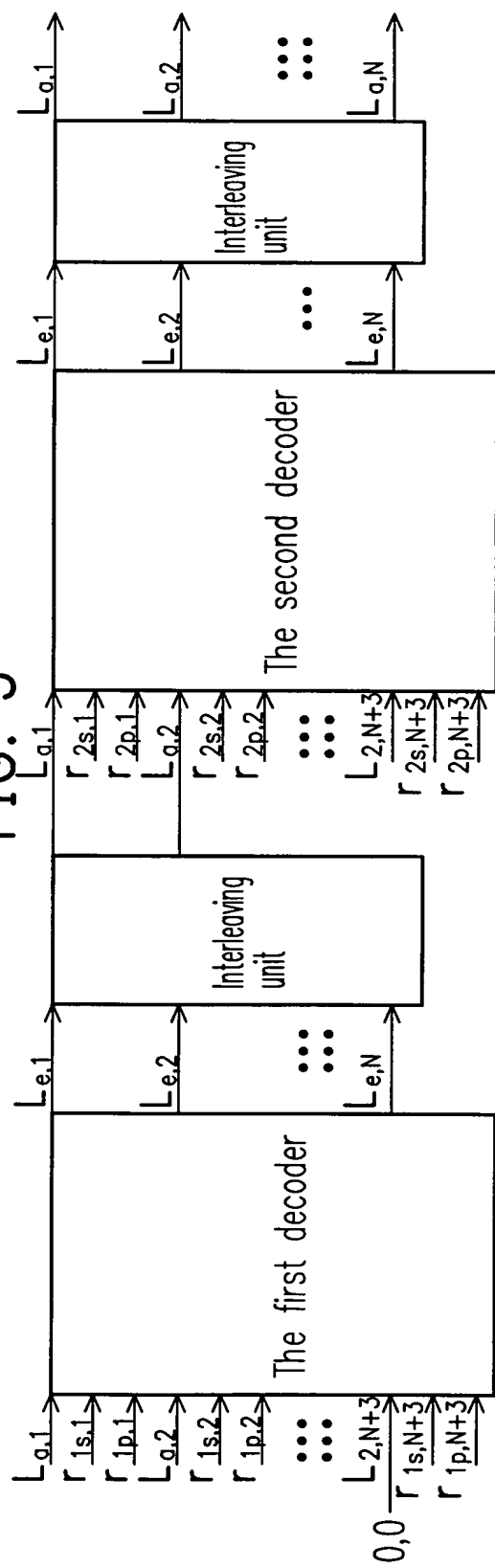


FIG. 3





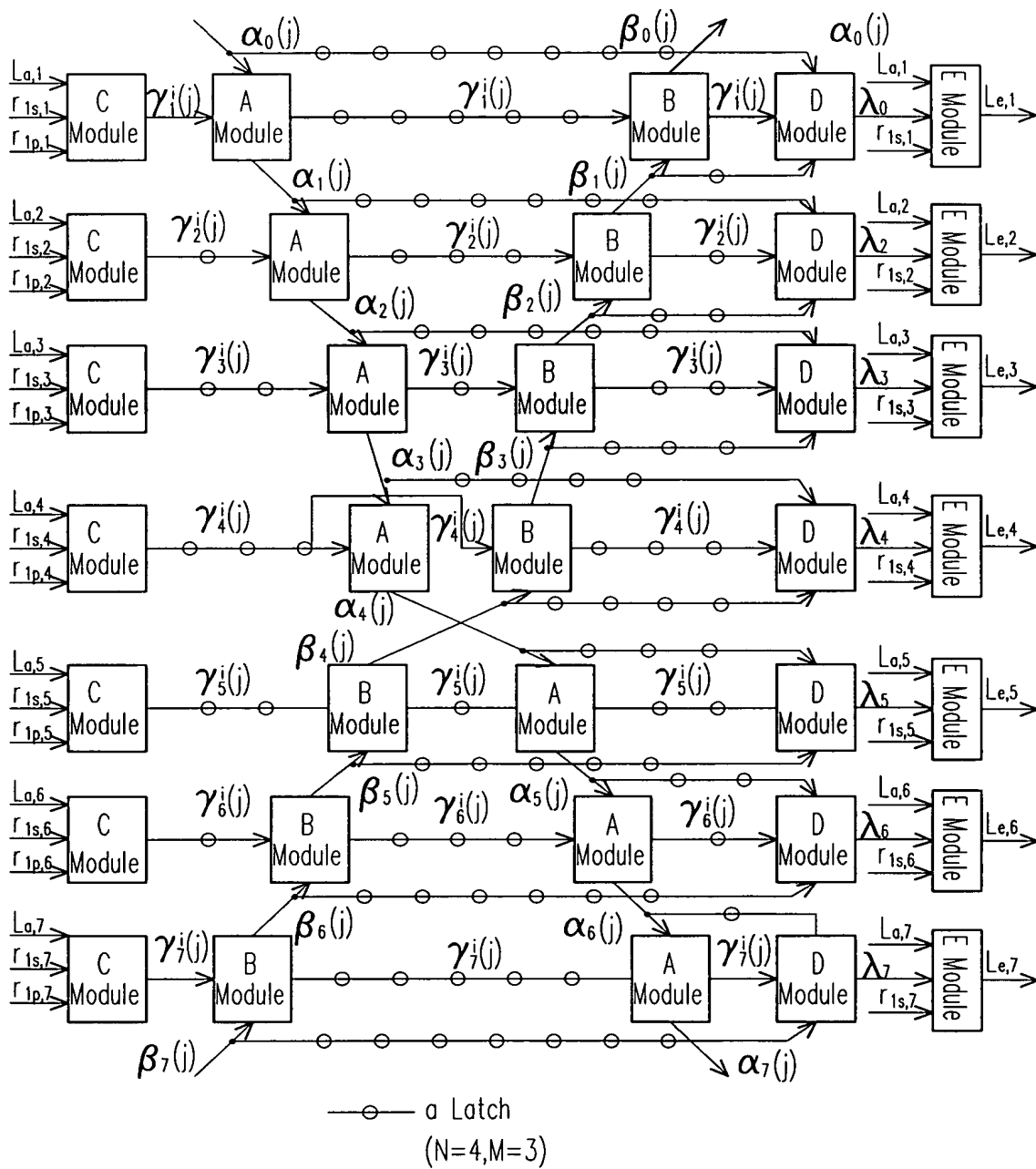


FIG. 6

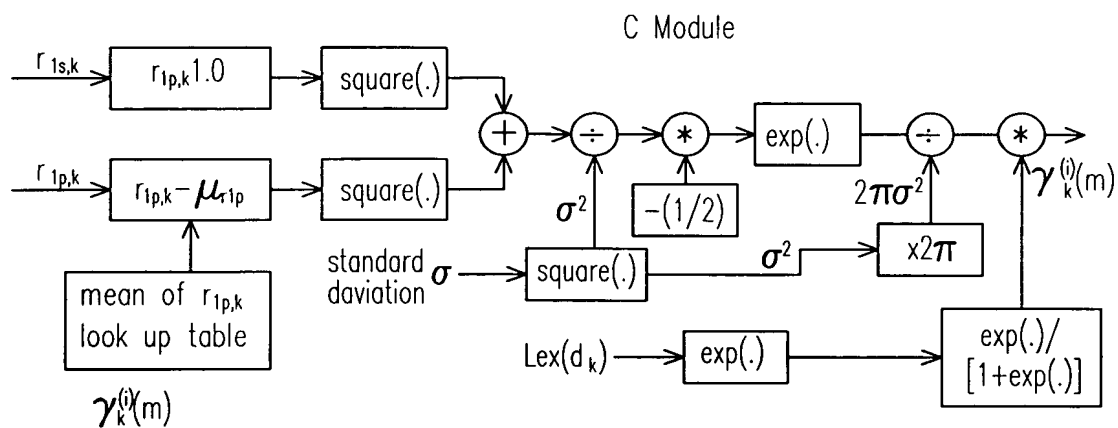


FIG. 7

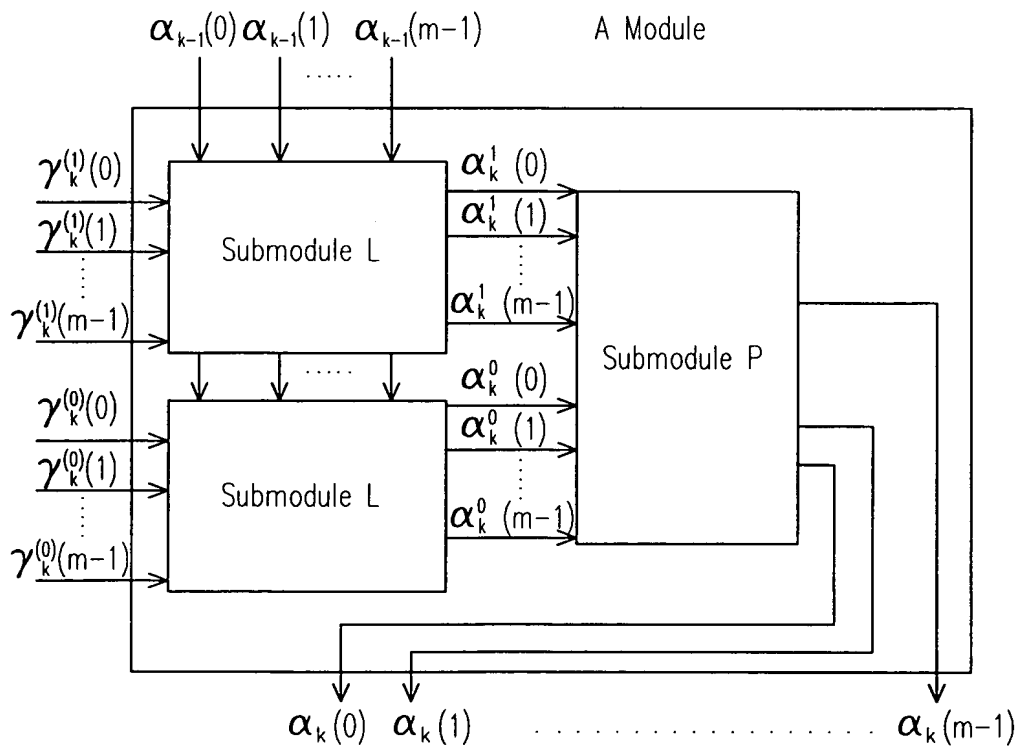
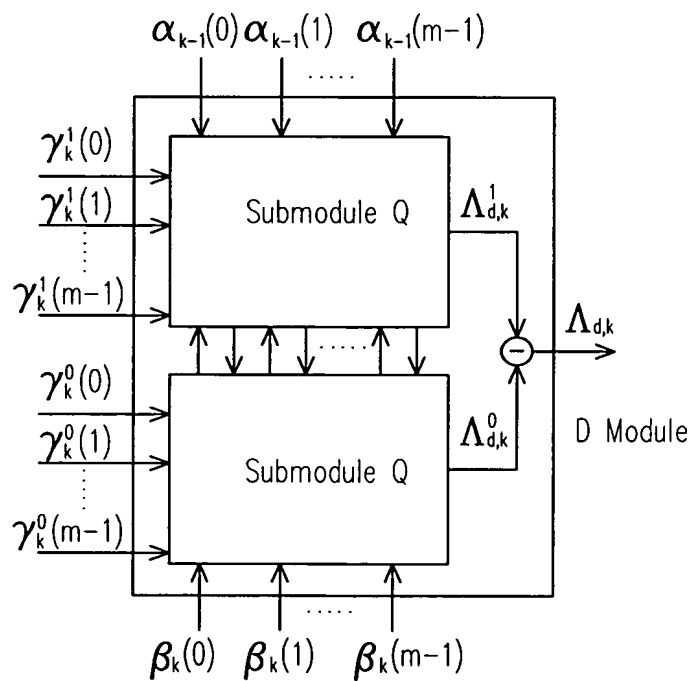
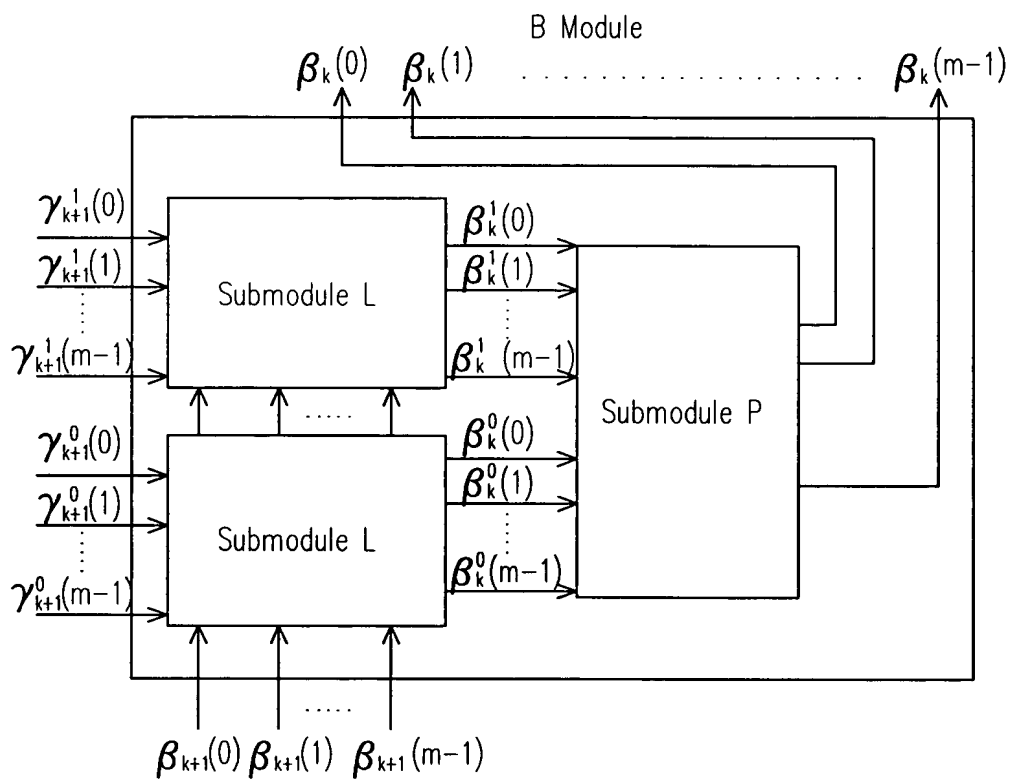


FIG. 8



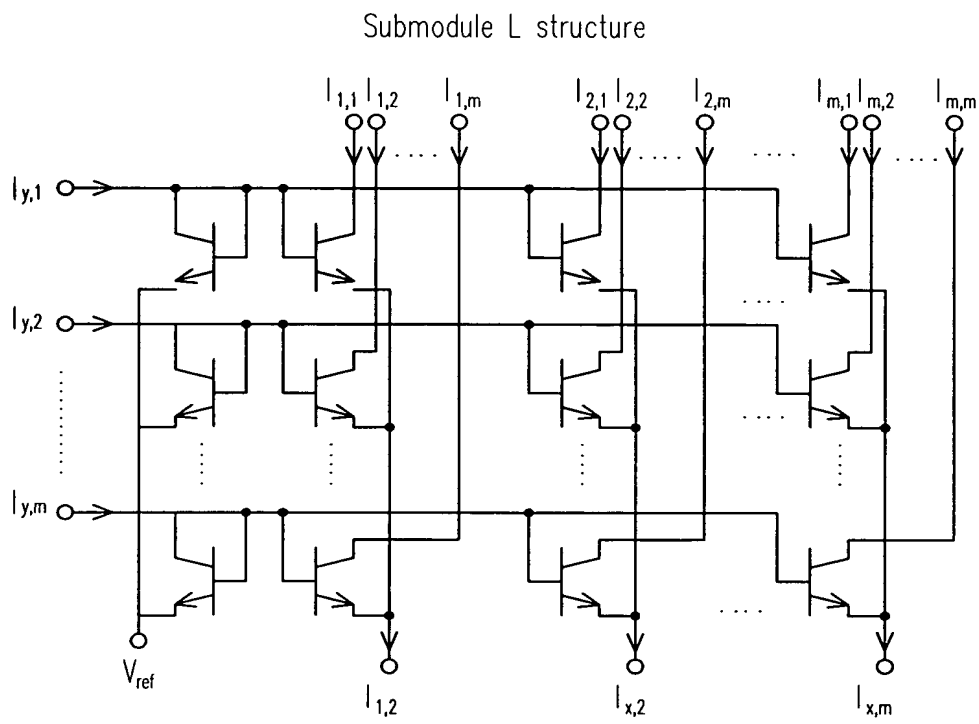


FIG. 11

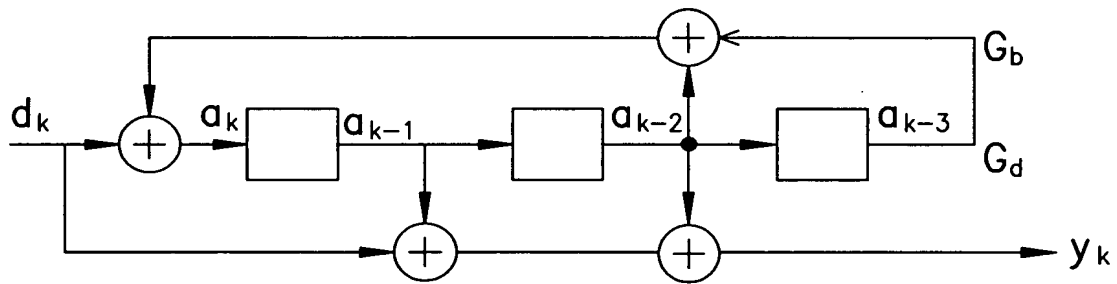


FIG. 12





FIG. 13

FIG. 14 is a block diagram of a digital signal processor (DSP) architecture. The architecture includes a multiplier (Mu) and a normalizer. The multiplier is used to calculate the product of two inputs, A and B, resulting in C = A \* B. The normalizer is used to normalize the output of the multiplier. The architecture is divided into two submodules, L and P, which are connected to a common bus. The bus is used to transfer data between the submodules and the multiplier. The architecture is designed to process digital signals in a parallel manner, allowing for efficient computation of the product of two inputs.

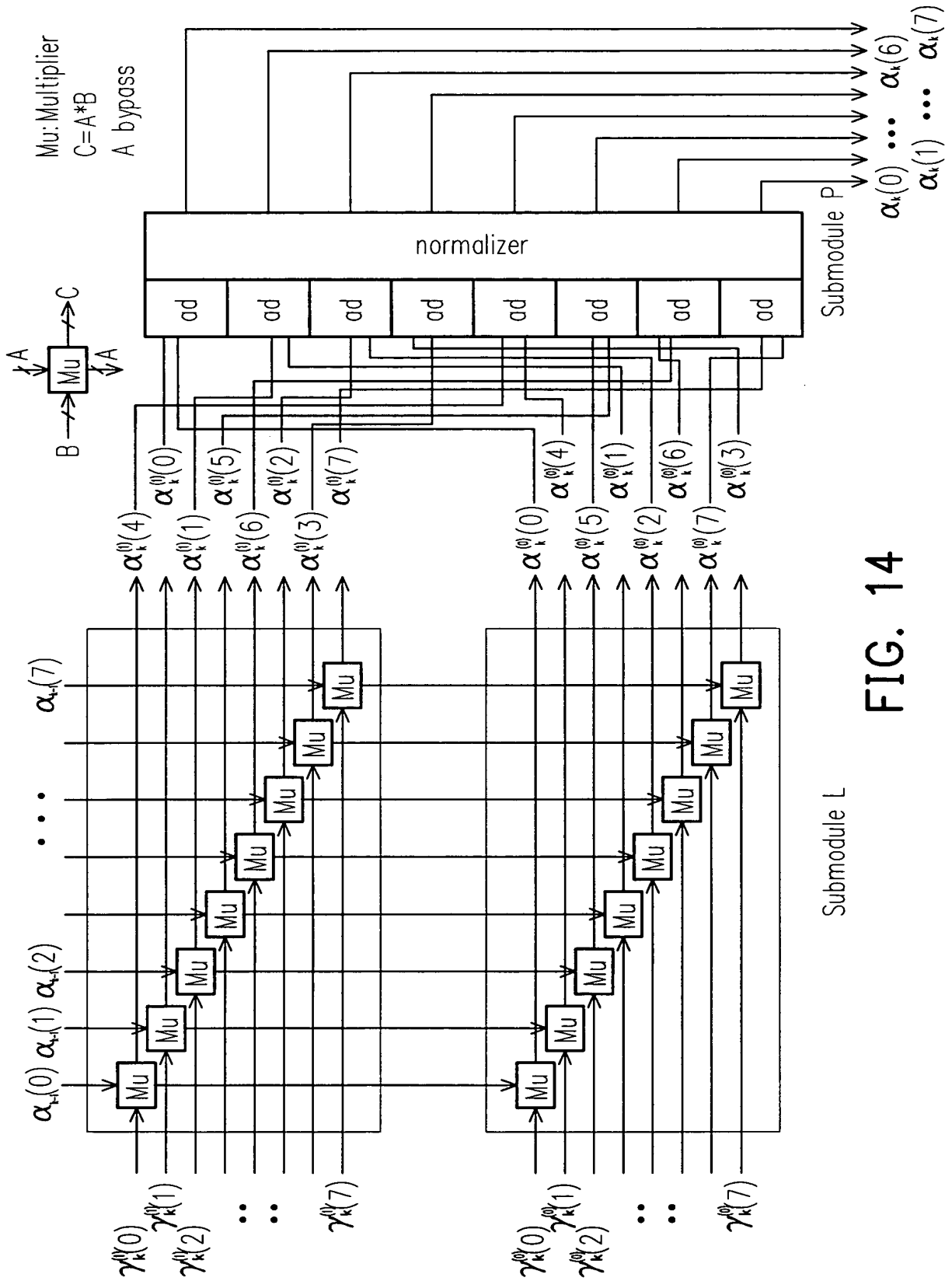


FIG. 14

$\alpha_{k-1}(0)\alpha_{k-1}(1)\alpha_{k-1}(2)$   $\dots$   $\alpha_{k-1}(7)$   
 $\gamma_k^{(1)}(0)$   $\gamma_k^{(1)}(1)$   $\gamma_k^{(1)}(2)$   $\dots$   $\gamma_k^{(1)}(7)$   
 $\beta_k(0)$   $\beta_k(1)$   $\beta_k(2)$   $\beta_k(3)$   $\beta_k(4)$   $\beta_k(5)$   $\beta_k(6)$   $\beta_k(7)$

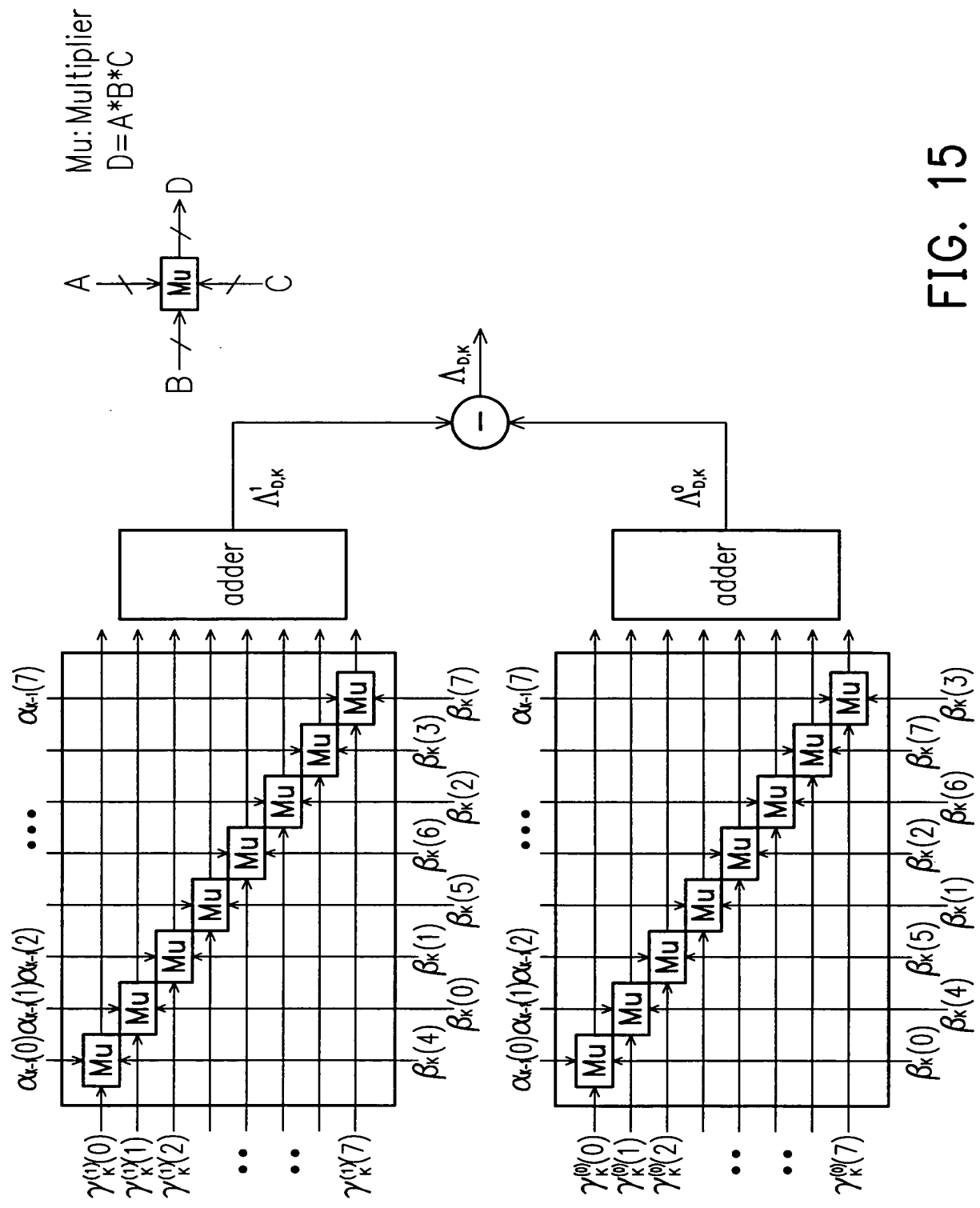


FIG. 15

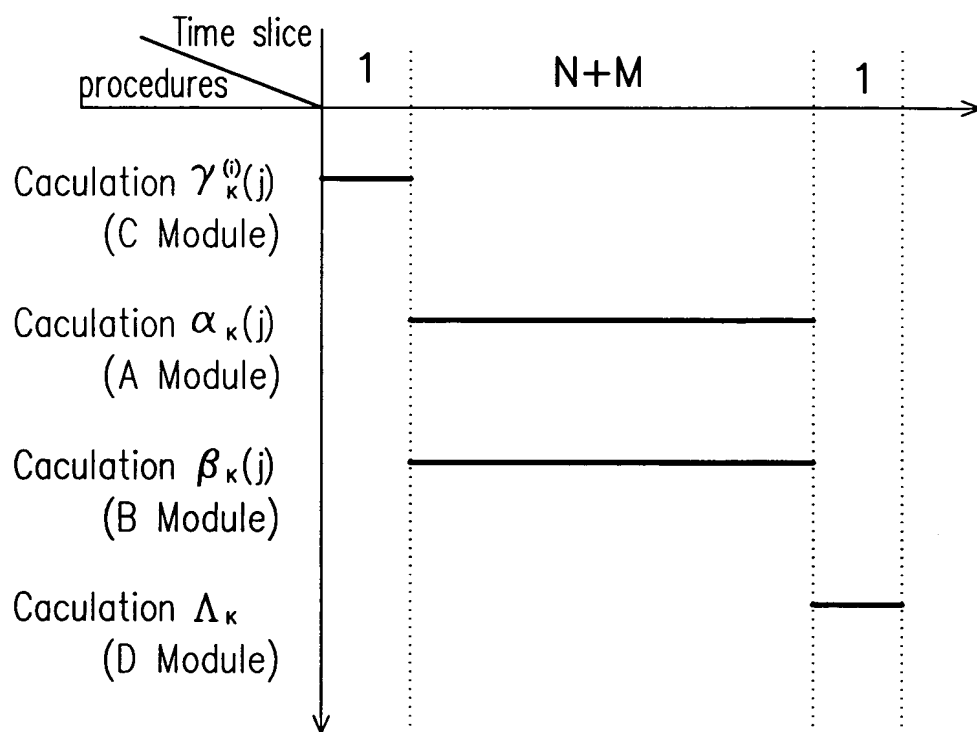


FIG. 16

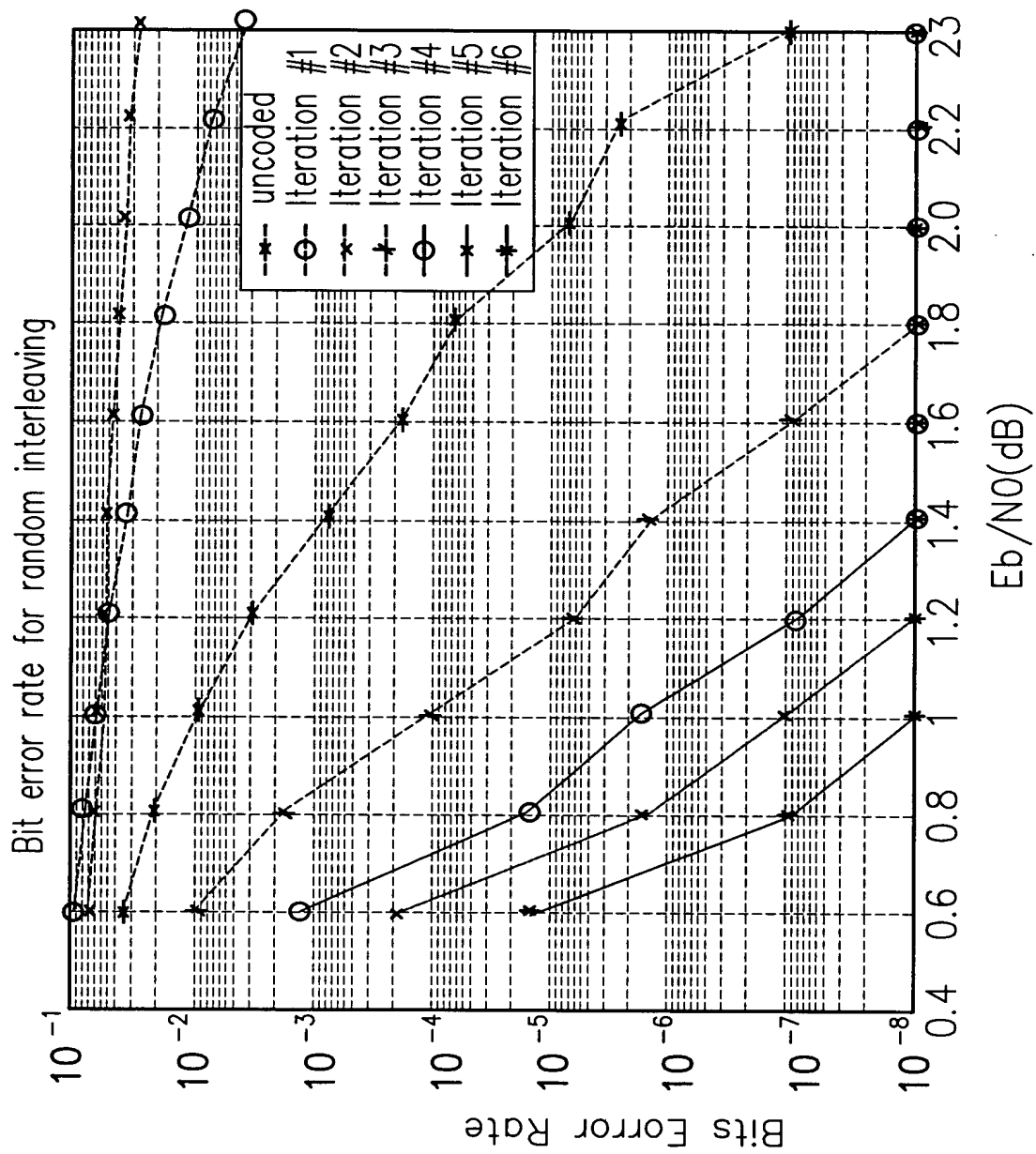


FIG. 17